We claim:

1. A method for connecting an integrated circuit chip to a circuit substrate, the integrated circuit chip including a bumped side having a plurality of conductive bumps, the method comprising the steps of:

applying adhesive directly to the bumped side of integrated circuit chip;

removing portions of the adhesive to expose contact regions of the conductive bumps, wherein the portions of adhesive are removed by softening the adhesive with a solvent and wiping the softened adhesive from the conductive bump; and

placing the bumped side of the integrated circuit chip against the circuit substrate such that the bumps provide for an electrical connection between the integrated circuit chip and the circuit substrate, and the adhesive forms a bond between the integrated circuit chip and the circuit substrate.

2. The method of claim 1, wherein after removing the portions of adhesive, the exposed contact regions of the conductive bumps have a rounded profile.

3. The method of claim 1, wherein after removing the portions of adhesive, the conductive bumps have heights greater than a thickness of the adhesive.

4. The method of claim 1, wherein a portion of the adhesive is removed to create an offset between the exposed contact regions of the conductive bumps and a primary exposed surface of the adhesive.

5. The method of claim 1, wherein the adhesive is applied to the integrated circuit chip by a technique selected from the group of coating the adhesive as a hot melt, coating the adhesive from solution, bonding the adhesive as a film in a lamination process, and pressing the adhesive as a film onto the bumped side of the integrated circuit chip.

6. The method of claim 1, wherein prior to removing the portions of adhesive, the conductive bumps have heights that are greater than a thickness of the adhesive.

7. The method of claim 1, wherein prior to removing the portions of adhesive, the conductive bumps have heights that are smaller than a thickness of the adhesive.

8. A method for manufacturing integrated circuit chips comprising the steps of:

providing a wafer including a bumped side having a plurality of conductive bumps;

applying adhesive to the bumped side of the wafer, such that the conductive bumps are over-coated with adhesive.;

softening the adhesive with a solvent;

wiping the softened adhesive from the tips of the over-coated conductive bumps to expose contact regions of the conductive bumps; and

dicing the wafer on which the adhesive has been applied into individual integrated circuit chips.

9. The method of claim 8, wherein after wiping the softened adhesive from the tips of the over-coated conductive bumps, the exposed contact regions of the conductive bumps have a rounded profile.

10. The method of claim 8, wherein the adhesive is applied to the wafer by a technique selected from the group of coating the adhesive as a hot melt, coating the adhesive from solution, bonding the adhesive as a film in a lamination process, and pressing the adhesive as a film onto the bumped side of the wafer.

11. The method of claim 8, wherein prior to removing the overcoat portions of adhesive, the conductive bumps have heights that are greater than a thickness of the adhesive.

12. The method of claim 8, wherein prior to removing the overcoat portions of adhesive, the conductive bumps have heights that are smaller than a thickness of the adhesive.

13. The method of claim 8, wherein after removing the overcoat portions of adhesive, the conductive bumps have heights greater than a thickness of the adhesive.

14. The method of claim 8, wherein after removing the overcoat portions of the adhesive, an offset exists between the exposed contact regions of the conductive bumps and a primary exposed surface of the adhesive.

15. The method of claim 8, wherein after the overcoat portions of adhesive are removed, and prior to dicing the wafer, a protective cover is placed over the adhesive and exposed contact regions.

16. An integrated circuit chip comprising:

a bumped side having a passivation surface on which a plurality of conductive bumps are disposed; and

a layer of adhesive that covers the bumped side of the circuit substrate, the adhesive having an primary surface that is substantially parallel to the passivation surface, and the conductive bumps having exposed contact regions that are not covered by the adhesive, wherein the exposed contact regions of the conductive bumps have a rounded profile.

17. The integrated circuit chip of claim 16, wherein the primary surface of the adhesive is polished.

18. The integrated circuit chip of claim 16, wherein the conductive bumps have heights greater than a thickness of the adhesive.

19. The integrated circuit chip of claim 16, wherein portions of the conductive bumps project outward from the primary surface of the adhesive such that a stand-off exists between the rounded profile of the conductive bumps and the primary surface of the adhesive.

20. A plurality of integrated circuit chips in wafer form comprising:

a bumped side having a passivation surface on which a plurality of conductive bumps are disposed; and

a layer of adhesive that covers the bumped side of the circuit substrate, the adhesive having an primary surface that is substantially parallel to the passivation surface, and the conductive bumps having exposed contact regions that are not covered by the adhesive, wherein the exposed contact regions of the conductive bumps have a rounded profile.

21. The plurality of integrated circuit chips in wafer form of claim 20, wherein the primary surface of the adhesive is polished.

22. The plurality of integrated circuit chips in wafer form of claim 20, wherein the conductive bumps have heights greater than a thickness of the adhesive.

23. The plurality of integrated circuit chips in wafer form of claim 20, wherein portions of the conductive bumps project outward from the primary surface

of the adhesive such that a stand-off exists between the rounded profile of the conductive bumps and the primary surface of the adhesive.

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